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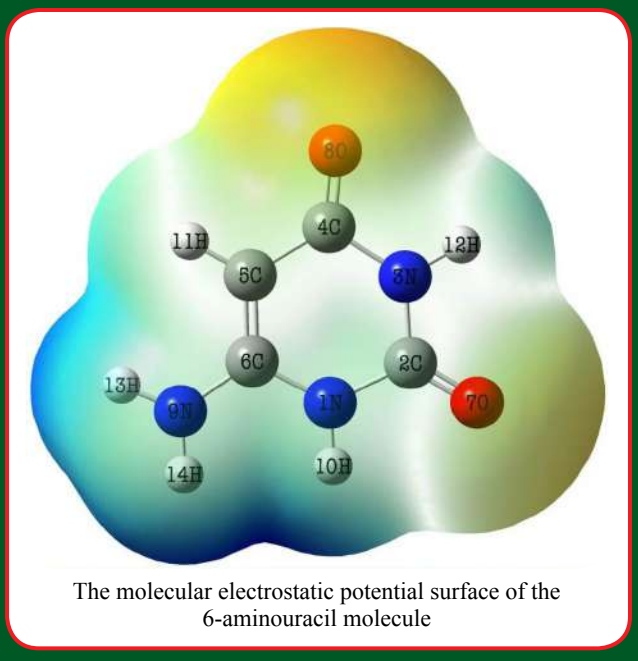

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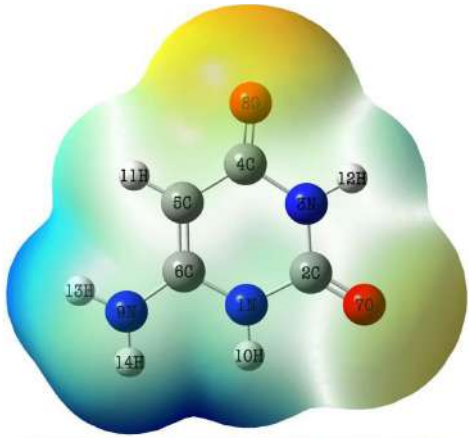

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Semiconductor devise having diffusion regions of reduced width

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A semiconductor memory device comprises active areas between isolation regions. Actives areas are isolated by isolation regions. An active area may include a diffusion region caused by ion implantation at the top proximate the substrate surface. The diffusion region has a diffusion region width that is larger than the active area width forming a mushroom shape. This will require an increased distance between two isolation regions and decrease the density of the formed memory device. A process is proposed to reduce the diffusion region width thus to substantially eliminate the mushroom effect.

Keywords: Semiconductor memory device, Diffusion region, Mushroom shape, Memory cells

1 Introduction

Memory devices are formed for various purposes including, for example, internal storage areas in computers, personal media players, cameras, and other electronic devices [1]. The term, "memory" identifies data storage that typically comes in the form of integrated circuit chips. In general, memory devices contain an array of memory cells for storing data, and row and column decoder circuits coupled to the array of memory cells for accessing the array of memory cells in response to an external address. One type of memory cell utilizes transistors capable of storing a charge. Such transistors typically comprise a pair of diffusion regions, referred to as a source and a drain, spaced apart and within a semiconductor substrate, such as a bulk single crystal silicon wafer. The transistors also include a gate provided adjacent to the semiconductor and between the diffusion regions for imparting an electric field to enable current to flow between the diffusion regions. In this paper, we describe a semiconductor devise having diffusion regions of reduced width as compared with devices reported elsewhere.

2 Diffusion region increase in width

Figure 1 is a schematic view of an example of a NAND Flash memory device [2]. As shown, the memory device includes a plurality of active areas forming an array, each active area, extending longitudinally along a substrate and separated from each other by isolation regions (e.g., shallow trench isolation (STI) regions). The active areas comprise a plurality of diffusion regions at least in regions between access lines, which are commonly referred to as wordlines. The wordlines extend across a plurality of the active areas and comprise control gates. The wordlines are grouped together in blocks that typically comprise 32 wordlines, although only 5 wordlines are shown in each of the two blocks illustrated in Fig 1 due to space limitations. On one side of each block is a gate configured as a drain select line, and on another side of each block is a gate configured as a source select line, each of which is configured to select a block of wordlines for reading from and writing to the memory device. A source slot can be at one end of a block and a plurality of data line contacts, such as bit contacts, are at an opposing end of each block. The bit contacts are coupled to the active areas and to a data line, such as bitline, of a plurality of data lines.

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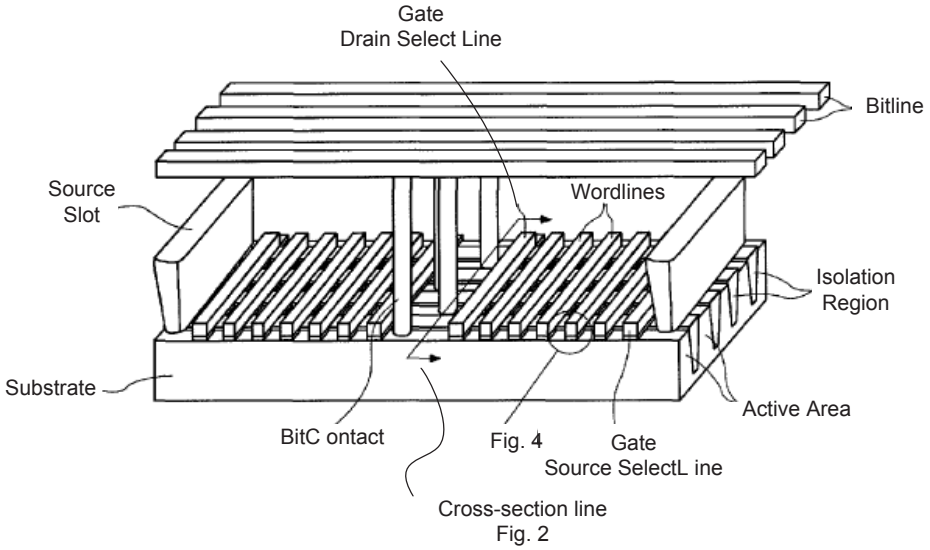

Fig. 1. An example of NAND Flash memory device.

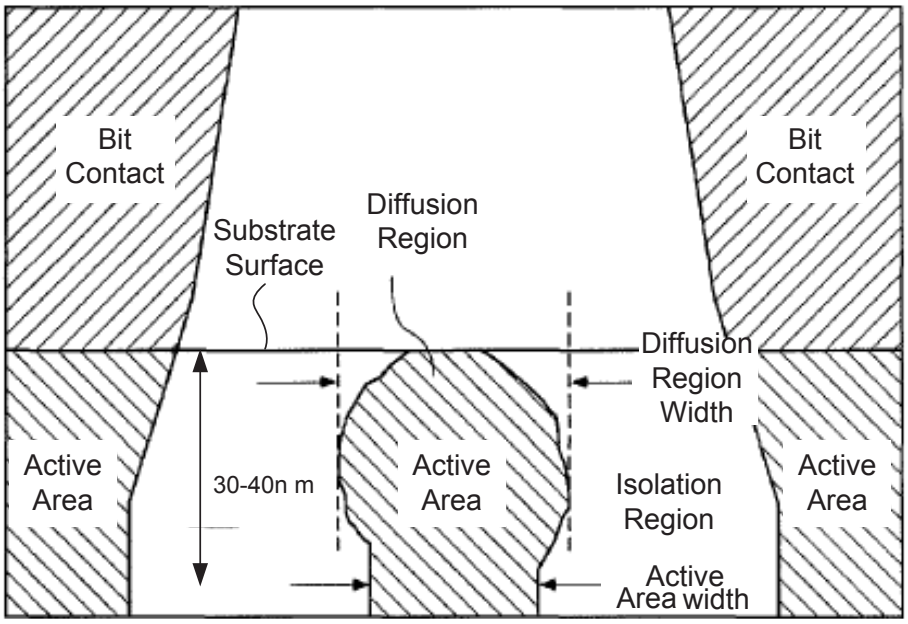

Fig. 2. Cross-section view of the memory device of Fig. 1 taken along cross-section line showing active areas of the memory device coupled to bit contacts.

Use of conventional processes to form a memory device, such as that shown in Fig 1, may result in an increase in the width of the diffusion regions at an end that is proximal to the substrate surface. For example, Fig 2 illustrates a partial cross-sectional view of the memory device of Fig 1 taken along a portion of cross-section line and showing a plurality of active areas of the memory device coupled to bit contacts. As discussed above, each of the active areas of the plurality of active areas is electrically isolated from other active areas by isolation regions, such as shallow trench isolation (STI) regions between the active areas.

The active areas have a width at a depth (e.g., about 30-40 nanometers or more) from the substrate surface. However, conventional active areas may also include a diffusion region comprising an end proximate the substrate surface having a diffusion region width that is larger than the active area width. Such an increase in width may be caused by, for example, unintended nucleation and growth of new crystals in the semiconductor material, and typically occurs during the manufacturing process.

The increase in width between the active area width and the diffusion region width at the end of the active areas proximate the substrate surface may also be referred to in this paper as a "mushroom" or "mushrooming." As used herein the term "mushroom" or "mushrooming" is intended to describe the nucleation and growth of new crystals in diffusion regions of a single crystal semiconductor substrate resulting in enlargement in width of the diffusion regions. Mushrooming becomes problematic as semiconductor devices are scaled to increasingly smaller dimensions. For example, the increase in width associated with the so-called "mushroom" can result in short circuits between active areas that are typically separated by STI regions, and present an obstacle in reducing the pitch between active areas in relation to reducing the overall size of semiconductor devices.

3 Mushroom effect

Methods for forming memory devices having reduced or substantially eliminated mushrooming will be discussed. Process flow of the method is illustrated in Fig 3, and the associated structures formed during the process are illustrated in Figs 4 through 8. Figure 4 is a cross-sectional elevation view of a portion of an N-channel transistor, such as one used to form a control gate, a drain select line or a source select line, of a semiconductor device during a stage of fabrication after several processing steps have occurred. Formation of the structure depicted in Fig 4 is well known and will not be detailed [3]. In general, a gate is formed adjacent to a semiconductor substrate, for example of silicon, such as a single crystal silicon substrate. For example, the gate may comprise N+ polycrystalline silicon (or "polysilicon") over the substrate, and separated by a gate oxide. The semiconductor device may include a spacer formed on lateral sides of the gate, and the substrate may include a plurality of halo implant regions and lightly doped drain (LDD) implant regions, such as the P halo and N-LDD region of an N-channel transistor formed in the substrate.

Referring to the first step in Fig. 3, an oxide, such as oxide layer (Fig 4), is formed over the gate and the substrate. The oxide layer may be formed as a screening oxide, which may serve to protect the substrate from residual ions on the surface of the substrate after ion implantation, as described in detail herein below. The oxide layer may comprise an oxide film such as silicon dioxide having an average thickness of about 15 nanometers. The oxide layer may be formed by conventional methods including, for example, chemical vapor deposition (CVD) using tetraethyl orthosilicate (TEOS deposition or furnace TEOS deposition). Prior to forming the oxide layer, the surface of the substrate may be cleaned.

In the second step in Fig 3, and with reference to Fig 5, ions are implanted into selected regions of the substrate completing the formation of the sources and drains. The ion implantation may comprise a relatively shallow implant of a large number (i.e., a high-dose) of ions to complete formation of the diffusion regions. The ion implantation is accomplished using known ion implantation equipment and techniques. Generally, a mask may be formed and patterned over the substrate, including the oxide layer, with a plurality of openings formed therein to selectively specify the locations for a plurality of the diffusion regions. An ion beam is directed at the substrate and the ions of the ion beam are provided with sufficient energy to cause the ions to penetrate through the oxide layer and to be implanted within the substrate to a shallow depth and with a high concentration to provide an excess of current carriers. As a result, the diffusion regions are electrically conductive. The ion beam may comprise Arsenic or BF2 (depending on whether it is an N-channel or P-channel transistor) and may be directed at the substrate at an energy level greater than about 30 KeV. The ion beam may be directed at the substrate at an energy level between about 50 keV and 60 keV. The mask

formed on the surface may be removed after the ions are implanted into the diffusion regions. The resulting structure after the second step may comprise of one or more diffusion regions formed in the substrate and adjacent to the gate. The diffusion regions may comprise the sources and drains of the transistors. Although Fig 5 illustrates a diffusion region on either side of the gate, according to various methods, one or more gates of a semiconductor device may comprise only a single diffusion region on one side thereof while other gates of a semiconductor device may only have the LDD regions and no diffusion regions adjacent thereto.

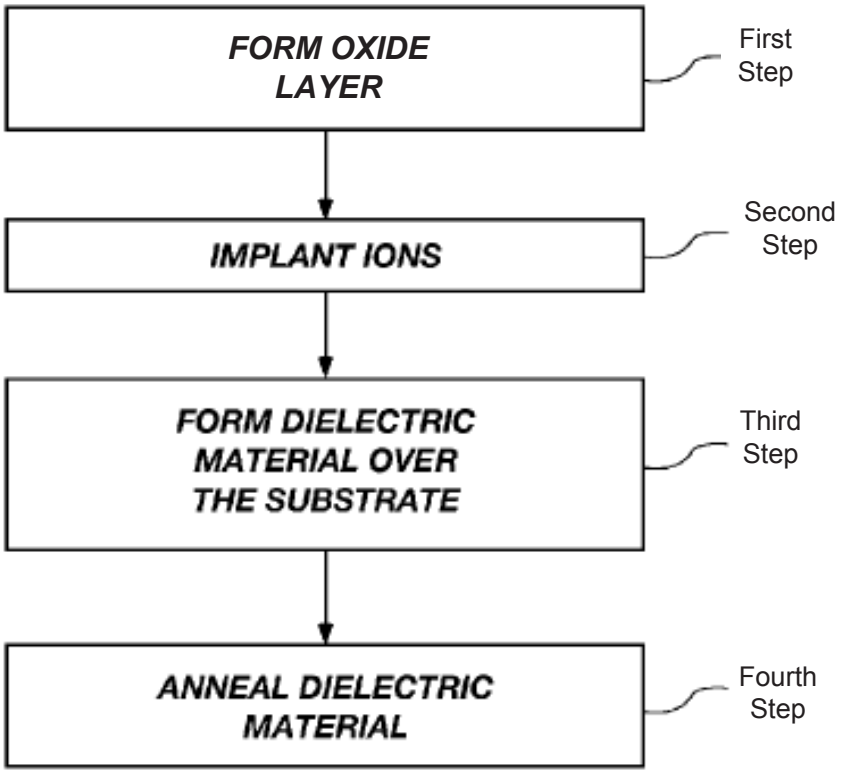

Fig. 3. Process flow of method for eliminating mushroom effect.

In the third step of Fig 3, a dielectric (Fig 6) is formed over the semiconductor substrate and the oxide layer. The dielectric is over the gates, and is over the semiconductor substrate between adjacent gates. Referring to Fig 6, an elevation cross-sectional view of the substrate is illustrated. The dielectric may be formed over and between adjacent gates to electrically isolate devices from each other. As used herein, a device may comprise a transistor including one or more diffusion regions having a gate adjacent the one or more diffusion regions. The dielectric may comprise a doped silicate glass, such as borosilicate glass (BSG), phosphosilicate glass (PSG), and borophosphosilicate glass (BPSG). The dielectric may be formed using, for example, a CVD process.

Figure 7 is an isometric sectional view of semiconductor device resulting from the foregoing processes as described herein with reference to Fig 3. The semiconductor device includes the substrate with a plurality of gates and a plurality of active areas comprising a plurality of diffusion regions between gates. The active areas are electrically isolated by shallow trench isolation (STI) regions between active areas positioned next to each other. The gates may comprise control gates located between a select gate drain at an end and a select gates source at another end. As set forth herein above, the semiconductor device further includes an

oxide layer and dielectric. As further shown in Fig 7, a plurality of openings may be subsequently formed in the dielectric down to the active areas. These openings may be filled with a conductive material to form a plurality of data line contacts, such as bit contacts, to couple certain diffusion regions to conductive data lines of the semiconductor device.

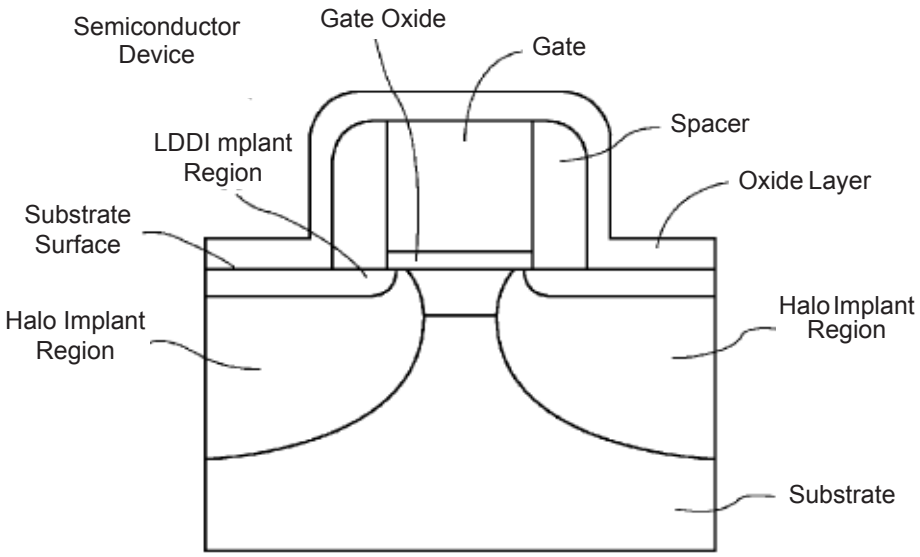

Fig 4. Cross-sectional schematic view of a portion of the memory device according to the first step of Fig 3.

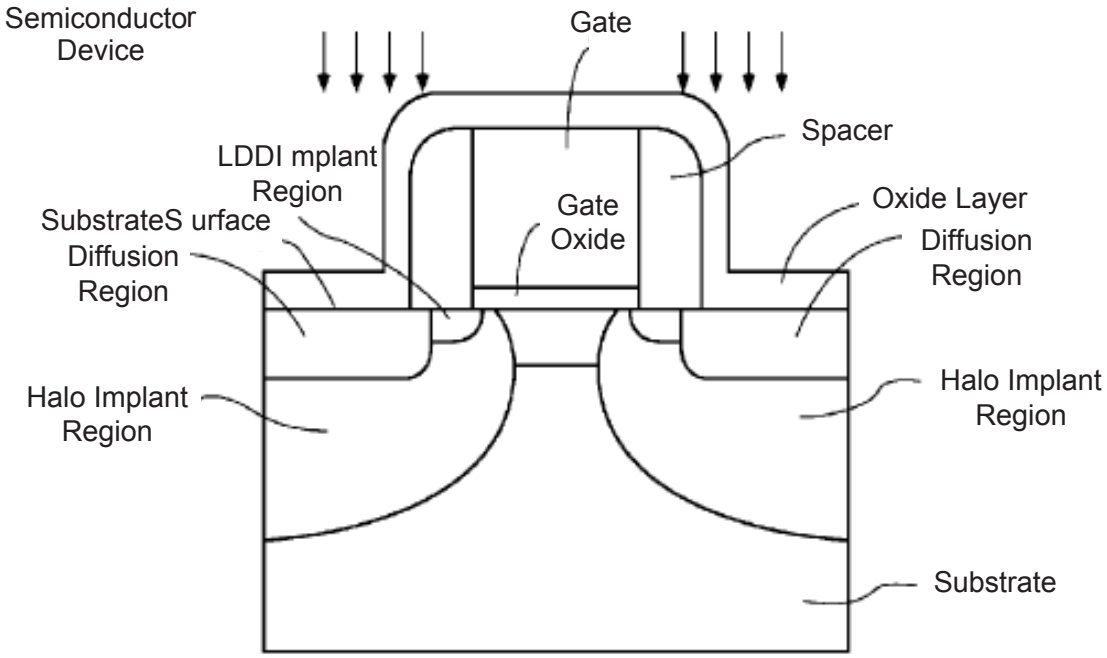

Fig 5. Cross-sectional schematic view of a portion of the memory device according to the second step of Fig. 3.

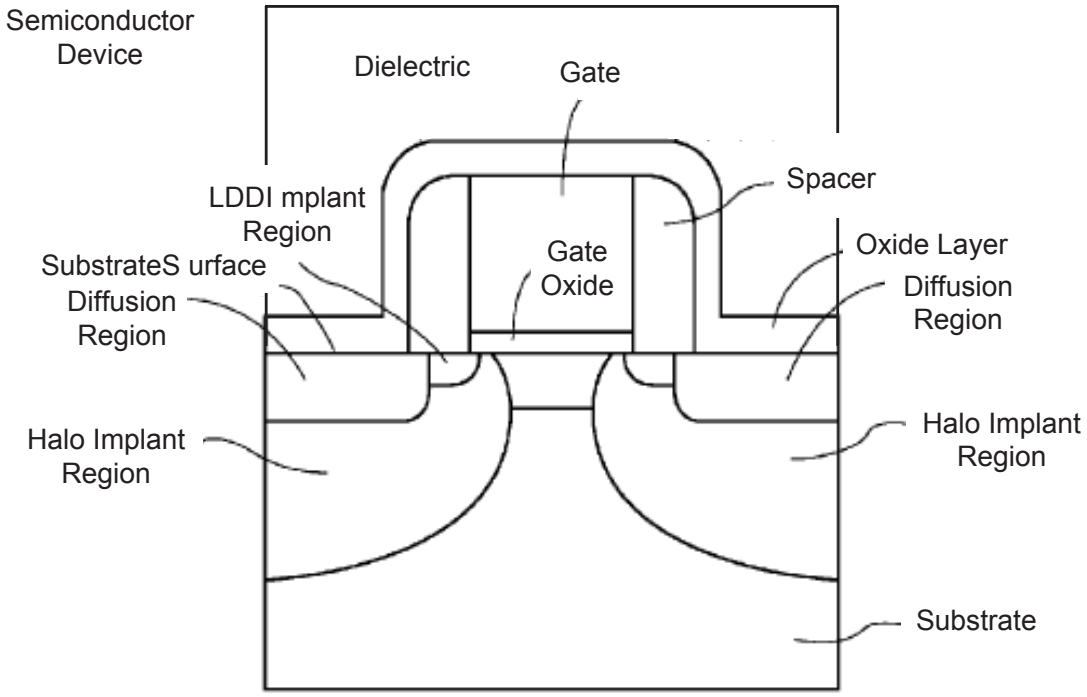

Fig 6. Cross-sectional schematic view of a portion of the memory device according to the third step of Fig 3.

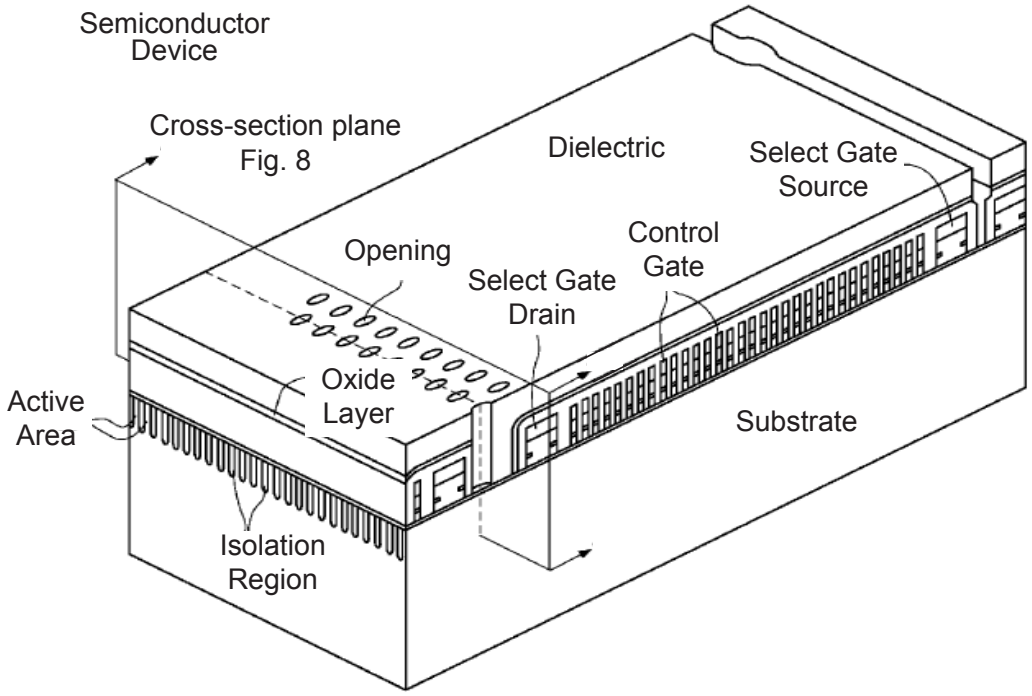

Fig 7. Semiconductor device having the substrate with a block of 32 wordlines and active areas that include diffusion regions between the wordlines.

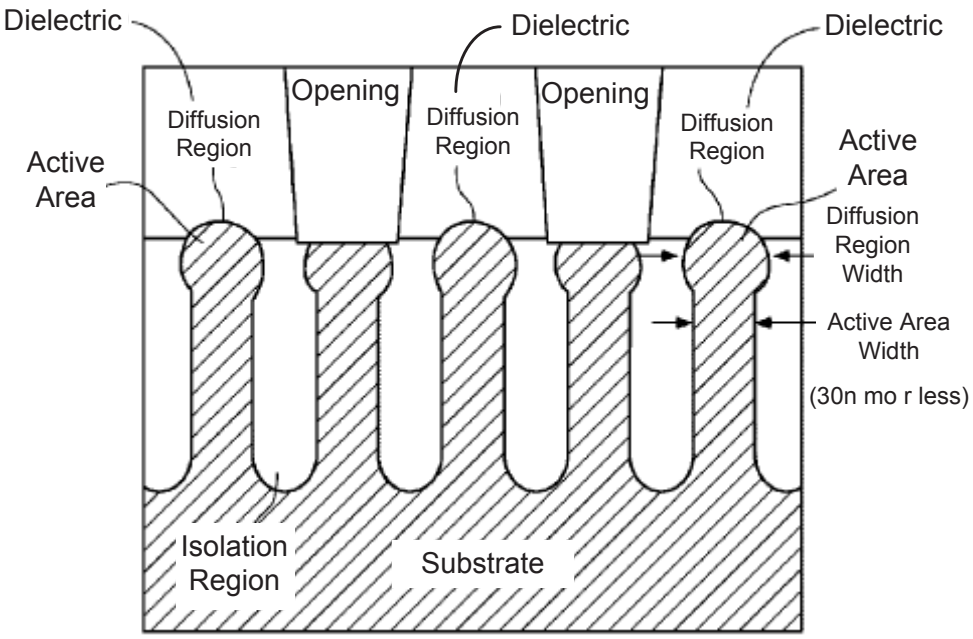

Fig. 8. Partial view of a cross-section of the substrate of Fig. 7 taken along the cross-section plane illustrating some of the active areas.

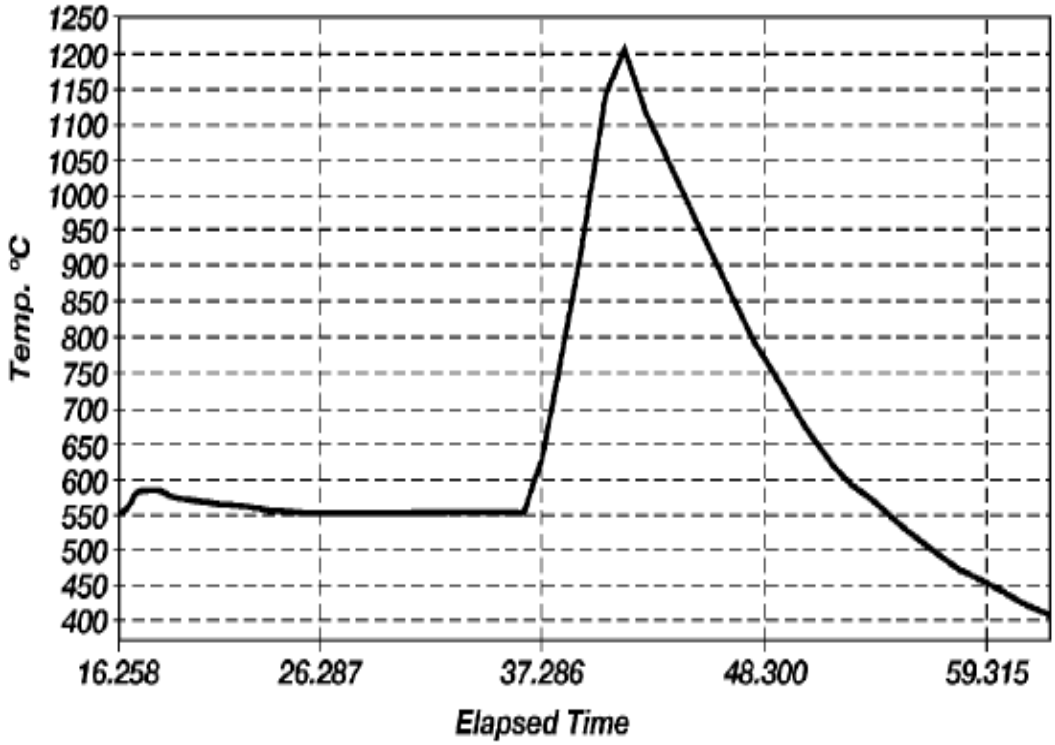

Fig 9. Graph of temperature (on the y-axis) as a function of elapsed time (on the x-axis) of annealing process according to the fourth step of Fig 3.

Figure 8 is a partial view of a cross-section of the semiconductor device taken through the cross-section plane of Fig 7 and illustrating some of the active areas. As used herein, the active areas refer to the portions of the semiconductor device that are separated by STI regions and include the diffusion regions, as well as a channel extending below the control gates. Employing the foregoing processes as described herein and in the order set forth in Fig 3 in which the oxide layer is formed prior to implanting the ions, the mushrooming described herein above may be reduced. For example, the active areas may have an average width of about 30 nanometers or less. The diffusion region width of the resulting mushroom may comprise an increase in width from the active area width of about 16.5% or less. The structure resulting from the fourth step in Fig 3 includes a semiconductor device having at least two diffusion regions separated by an STI region such as, for example, a memory device having an array of diffusion regions in the active areas. At least two diffusion regions of the semiconductor device have an increase in width at a proximal end of about 16.5% or less from the active area width. In other words, at least two diffusion regions comprise a first width or active area width at a depth (e.g., about 30-40 nanometers or more below the surface) within the substrate (referred to herein as the original width, since it is a width of the diffusion regions when they are initially formed) and a second width or diffusion region width near the substrate surface (referred to herein as the diffusion region width of the resulting mushroom), wherein the second width is about 16.5% greater or less than the first width.

For comparison, if the first step and the second step in Fig 3 are exchanged, the second width is about 40% greater or less than the first width.

4 Eliminating mushroom effect

In the fourth step of Fig 3, the dielectric may also be subjected to a high temperature annealing process, such as to densify the dielectric, as well as to activate the ion implants and remove damage induced by the ion implantation in the substrate. For example, using BPSG for dielectric, the BPSG material is annealed after being formed over the substrate. An annealing process for BPSG may include utilizing rapid thermal processing (RTP) or a furnace annealing process. Such an annealing process may include exposing the BPSG to temperatures of about 650^{o} C. for a relatively short time period such as, for example, 10 minutes.

The semiconductor device may be exposed to processing steps for reducing nucleation of the substrate material and for enhancing grain growth of the substrate material. For example, the fourth step of Fig 3 may comprise an annealing process for the dielectric, the annealing process configured to promote grain growth, rather than nucleation, of the substrate material. The annealing process may comprise a temperature spike annealing process in which the temperature is ramped up to a peak temperature and then reduced from the peak temperature without any significant delay. The temperature spike annealing process may utilize a Rapid Thermal Process (RTP) in which the dielectric is exposed to a first temperature for a period of time sufficient to stabilize the temperature of the semiconductor device. The temperature is then rapidly ramped up to a substantially greater peak temperature that will more favorably promote growth of existing grains instead of nucleation of new grains. Once the temperature reaches the peak temperature, the temperature is quickly lowered to a substantially lower temperature. The peak temperature is a temperature greater than about 1,050° C. By way of example, the peak temperature may be between 1,050° C and 1,200° C, which may be held for about two seconds or less.

Figure 9 illustrates a graph depicting the temperature on the y-axis and an elapsed time on the x-axis for a modified annealing process. As illustrated, the dielectric is exposed to a temperature between about 550° C and 600° C for an initial period of time. For example, the dielectric may be exposed to a temperature between about 550° C and 600° C for less than about one minute. The temperature is then ramped up at a relatively rapid rate to about 1,200° C over the course of about five seconds (e.g., at an average rate of about 125° C per second). Once the temperature reaches the peak temperature, 1,200° C in this example,

the temperature is lowered. For example, the temperature is lowered to between about 400° C and 700° C at either a controlled or uncontrolled rate. The device may then be transferred to another cooling stage in room air to further cool to room temperature.

5 Concluding remarks

Employing the processes described herein as set forth in Fig 3, and the annealing process described with reference to Fig 9, described in Section 3 and shown in Fig. 8 may be substantially eliminated. For example, the diffusion region width (Fig 8) at the proximal end of the substrate material may comprise substantially no increase in width, such that the entire longitudinal length thereof has a substantially constant average width. The resulting structure includes a semiconductor device having one or more diffusion regions such as, for example, a memory device having an array of diffusion regions. The diffusion regions of the semiconductor device have substantially no increase in width at a proximal end from the average width. In other words, the diffusion regions comprise a first width (e.g., active area width) and a second width (e.g., diffusion region width) that are substantially equal (e.g., there is no mushroom).

An electronic system, such as a computer system, may comprise an input device, an output device, and a memory device each electrically coupled to an electronic signal processor. As used herein, the computer system includes not only computers such as personal computers and servers, but also wireless communication devices (e.g., cell phones, personal digital assistants configured for text messaging and e mail), cameras, chip sets, set top boxes, controllers, vehicle and engine control and sensor systems, digital music players, and other combinations of the above-referenced input, output, processor and memory devices. The memory device, e.g., the semiconductor device discussed above, comprises of two or more diffusion regions comprising a width of about 30 nanometers or less. The memory device may comprise any conventional programmable memory device, such as a Flash memory device or a CMOS memory device.

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