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Surface ion trap for barium ion - the industrial way

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Ion trap is the fore-runner in the field of quantum information, communication and computation.Therefore, miniaturization and integration of these devices forms an important field of research towards making this technology scalable. The most scalable architecture of an ion trap processor is a surface trap design. Technologically, there exists well developed commercial techniques for micro-fabrication. However, the goal of this article is to explore to what extent these commercial approaches can be directly implemented in developing planar surface ion traps.

Keywords: Ion trap, Quantum information, Cryogenic cooling

1 Introduction

Ion traps play an important role in developing technologies harvesting quantum nature of small particles. This has led to the promising field of quantum computation, information [1-3] and communication [4]. In a realistic quantum computer, it is essential to have more than 100 quantum bits or qubits to surpass the capabilities of any present day machine [5]. However, this requires much more scalable approach than is presently available with linear ion traps. These extensively used ion traps are three dimensional electrode arrangements so as to confine ions in all 3-dimensions with one of the dimension being weaker confinement as compared to the other two. Such a trapping arrangement leads to one dimensional qubit arrangement and hence difficult to scale up. Alternatively, ions can be trapped above a surface electrode structure [6-7] which can then be shuttled around from processor to memory units [8,9].

Here we will explain several design, simulation and fabrication of surface electrode ion traps to trap Ba^+ ion using the standard industry processes. Surface traps consists of radio frequency (RF) and direct current (DC) electrodes all lying on a plane. It offers advantages in terms of scalability, shorter fabrication time and greater laser accessibility. But, its low trap depth and shorter ion-electrode distance makes it challenging in terms of storage time and higher heating rates. It requires special attention for its design and fabrication specially in terms of surface contamination [10]. Recently, it was found that the use of cryogenic cooling of the trap surface reduces the heating rate by almost two orders of magnitude [13,14]. Another alternate method of using argon ion mill to clean the surface is seen to reduce the heating rate by two orders of magnitude [10]. Actual reason of this heating mechanism is not that well known, however what is mostly believed is that contamination leads to patches on the electrode surfaces [11,12]. These insulating patches modify the potential and in case of applied RF these modifications lead to time varying field on top of the conning field. Since the trapping potential is low in case of planar geometry, these modifications lead to increased noise and the ion is eventually heated out of the trap. Still a lot of efforts need to be made to understand this heating rate in a surface traps as these architecture promises 2-dimensional arrangement of qubits and hence easy to

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implement quantum codes like the surface codes [15]. Several different designs and fabrication techniques have been tested to trap Ba^+ on a surface electrode trap. In the following section we review different types of surface ion traps that has been designed and fabricated in our laboratory. The review starts with simulation techniques for designing a surface planar ion trap followed by a detailed description of our experimental setup. The results of testing industrially prepared traps and their limitation are discussed in the penultimate section followed by the brief description of alternative approaches and conclusion.

2 Simulation of trapping potential

Trap simulations involve calculation of electric potential (ϕ) due to a charge distribution around the position of the ion. Most of the surface trap geometries are complex enough to solve it analytically. Very few specific cases can be solved analytically. The analytic solution for traps with five wire geometry has been presented in references [16-19]. Here, we will present the numerical simulation of the surface electrode geometries to get a stable trapping potential. Numerical methods involve ways to solve the Laplace equations of a boundary value problem for a particular geometry. The governing equation for any trap geometry is the Laplace equation in free space

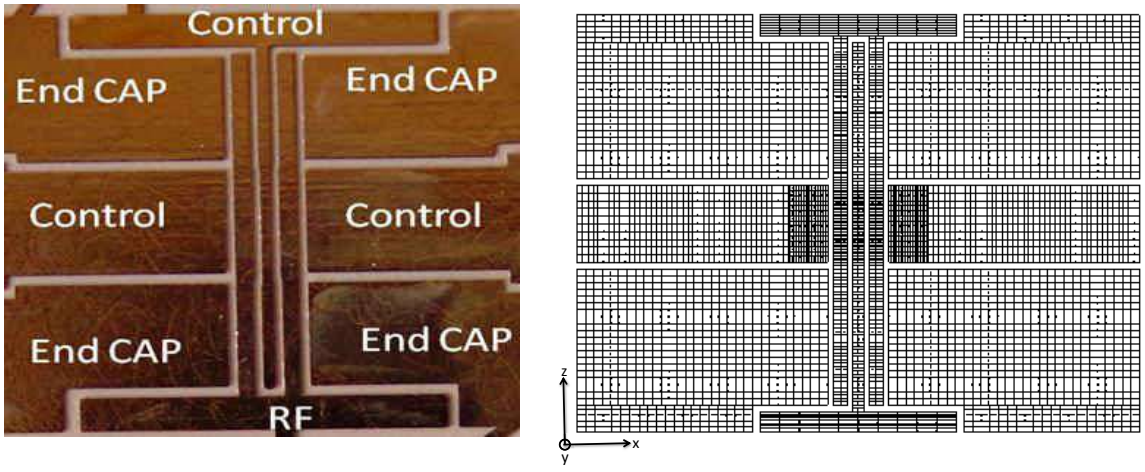
$$\nabla^2\phi = 0 \tag{1}$$

where, the Dirichlet boundary conditions

$$\phi_i = U_i \quad i = 1, 2...n \tag{2}$$

ϕ_i is the surface potential due to the i^{th} electrode and U_i is the voltage applied to it.

There are two commonly used method to numerically solve partial differential equations, the finite element method (FEM) and the boundary element method (BEM) [20,21]. In FEM the volume for which one wants to know the solutions is divided into small but finite size elements with uniform material properties, while in BEM only the boundary is discretized. We performed the trap simulations using BEM because a rectangular grid structure can be chosen for solutions. This helps to post process with matrix based programming languages like MATLAB.



(a) (b)

Fig 1. (a) Trap electrodes with their designations in a five wire geometry. (b) subdivisions of the pcb geometry in CPO. The central dense sub-divisions are made to increase the accuracy of the simulation. Boundary element method (BEM) has been employed for the simulation.

Trap simulations has been performed using the charged particle optics (CPO®) package which uses boundary element method for simulation. The trap is drawn in a computer aided design (CAD) program and pre-segmented into rectangular parts before put into CPO. The CPO further segments each part into finer mesh structure. Figure 1 shows typical design of a five wire segmented surface trap electrodes and its CPO image with grid structure. The grid size near the trap center is chosen to be finer as compared to other parts to get more accurate results. With a relatively large grid size, the trap center is first coarsely located. Then using a finer grid size at the central trapping region helps to calculate the accurate potential near the trap center within shorter simulation time. In the following, we will concentrate on the radiofrequency and DC potential simulation separately as they require different sets of approach to numerically solve them.

A. RF Potential

In an ion trap, confinement in the radial directions is achieved by application of radio frequency voltage to the central RF electrodes as shown in Figure 1. The time dependent potential caused by the RF electrodes can be represented by an effective time independent pseudopotential [22]. The simulation process involves setting up all the DC electrodes to 0 V, while the RF electrode to 1 V. Calculated ϕ_{RF} from CPO is post processed in MATLAB to get the pseudopotential ψ_{RF} using the following formula

$$\psi_{\mathrm{RF}} = \frac{e^2}{4m\,\Omega_{RF}^2} |\nabla \phi_{\mathrm{RF}}|^2$$

where e represents electric charge and m represents mass of the ion. Figure 2 shows typical cross section of the RF pseudopotential obtained from CPO simulation for a five wire segmented surface trap design. As the contour lines indicate there is a minimum at about 400 μm above the surface. If the ion moves further up, it will encounter contour lines which are not closed and hence goes out of the trap. The difference of the potential between the minimal value contour (not necessarily zero) to the escape point contour is about 100 meV.

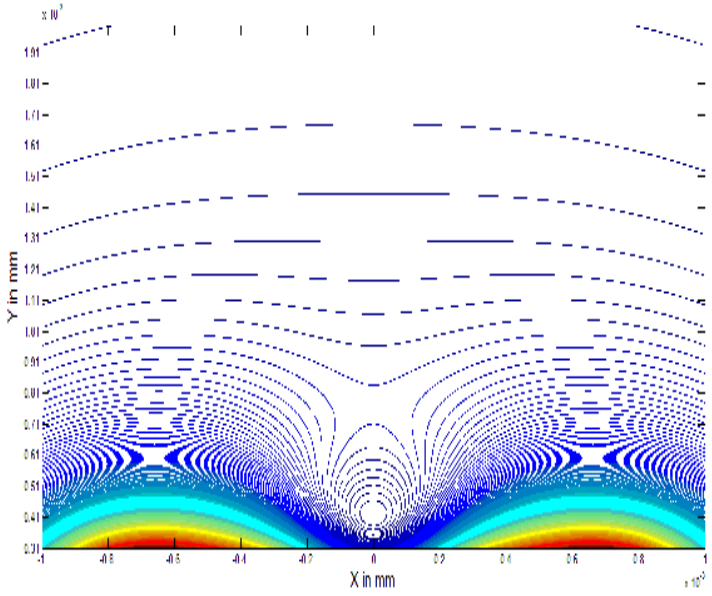


Fig 2. RF pseudo potential cross section calculated from the potential calculated using CPO and then post processed in MATLAB

B. DC Potential

The radio frequency voltage applied to the central RF electrodes ensures trapping potential in radial directions. The axial trapping potential is created by DC electrodes symmetrically placed on both sides of the RF electrodes. Simulation of the DC potential can be applied to any electrode configurations. This is justified by the linear nature of the involved differential equation and the principle of superposition of potentials. The general approach to calculate the DC potential at any arbitrary point (r_k) above the trap surface is the following:

1 RF electrodes are set to zero potential.
2 Assign U_i to unit voltage whereas rest $U_{j\neq i}$ is set to 0 V.
3 Base function $\phi_i(r_k)$ is calculated at all grid points.
4 Steps 2 and 3 are repeated for all the DC electrodes present.
5 Total DC potential is calculated from the weighted sum of all the individual potentials for each electrode.

Therefore, we obtain

$$\Phi_{DC} = \sum_{i=1}^{n} U_i \phi_i(r_k). \tag{3}$$

This allows the flexibility of optimization by only varying the applied voltages instead of solving the Laplace equations every time.

C. Multipole potentials

To obtain a stable trapping and for certain precision measurements, a near harmonic potential must be obtained near the trap center. In general the potential created by each electrode can be expanded into a sum of multipole potentials [23]. To explain it more clearly the potential for j^{th} electrode upto the second order in Cartesian coordinates can be written as

$$\Phi_j = C_{0,j} + C_{1,j}x + C_{2,j}y + C_{3,j}z + K_{4,j}(x^2 - y^2) + C_{5,j}(2z^2 - x^2 - y^2) + C_{6,j}xy + C_{7,j}yz + C_{8,j}zx \tag{4}$$

where $C_{i;j}$ are the constant pre-factors. Now from superposition principle the total potential at the trap center can be written as a linear sum of the potentials created by individual electrodes. After performing the sum over all electrodes j, the multipole moments can be expressed by matrix $C_{i;j}$, where j denotes the electrode number and i denotes the multipole component in the expansion. For a set of voltages U_i the multipole moment M can be evaluated by multiplying $C_{i;j}$ with the U_i as

$$\begin{bmatrix} \mathrm{M}_1 \\ \mathrm{M}_2 \\ \mathrm{M}_3 \\ \cdot \\ \cdot \\ \cdot \\ \mathrm{M}_k \end{bmatrix} = \begin{bmatrix} C_{1,1} & C_{1,2} & \cdot & \cdot & \cdot & C_{1,\mathrm{N}} \\ C_{2,1} & C_{2,2} & \cdot & \cdot & \cdot & C_{2,\mathrm{N}} \\ C_{3,1} & C_{3,2} & \cdot & \cdot & \cdot & C_{3,\mathrm{N}} \\ \cdot & \cdot & \cdot & & & \cdot \\ \cdot & & & \cdot & & \cdot \\ \cdot & & & & \cdot & \cdot \\ C_{k,1} & C_{k,2} & \cdot & \cdot & \cdot & C_{k,\mathrm{N}} \end{bmatrix} \begin{bmatrix} U_1 \\ U_2 \\ U_3 \\ \cdot \\ \cdot \\ \cdot \\ U_{\mathrm{N}} \end{bmatrix}$$

where N denotes the total number of DC electrodes and k denotes the number of terms considered in the expansion. The monopole term corresponds to a constant offset so it has been neglected. Our target is to get the multipole potential reduced to only one of the terms in the expansion. To illustrate it in detail if one is interested in generating an x-dipole, the requirement is to find a set of $U_i s$ so that only the first term on the left hand side of the above equation has nonzero value.

$$\begin{bmatrix} 1 \\ 0 \\ 0 \\ . \\ . \\ . \\ 0 \end{bmatrix} = \begin{bmatrix} C_{1,1} & C_{1,2} & . & . & . & C_{1,N} \\ C_{2,1} & C_{2,2} & . & . & . & C_{2,N} \\ C_{3,1} & C_{3,2} & . & . & . & C_{3,N} \\ . & & . & & & . \\ . & & & . & & . \\ . & & & & . & . \\ C_{k,1} & C_{k,2} & . & . & . & C_{k,N} \end{bmatrix} \begin{bmatrix} U_1 \\ U_2 \\ U_3 \\ . \\ . \\ . \\ U_N \end{bmatrix}$$

Usually C is a rectangular matrix unless the number of terms in the expansion equals to the number of DC electrodes. The solution has to be found numerically by least squares approximation. This involves solving the equation $M = CU$ by minimizing the norm

$$||CU - \boldsymbol{M}||$$

This is done in MATLAB by calculating the pseudo inverse using singular value decomposition method.

The total potential is calculated by summing the RF pseudopotential (ψ_{RF}) and the DC potential (Φ_{DC}).

$$\psi = \psi_{RF} + \Phi_{DC}$$

Usually the simulated potential and the actual required potential agree within 10%, the discrepancy is mainly due to the presence of stray fields which are not possible to model in the experiment. Once the simulation results are obtained, the trap is fabricated by different micro-fabrication methods. In the following a detail of the experimental setup required to trap and laser cool a barium ion is described.

3 Experimental setup

In order to trap and laser cool Ba^+ a few steps are required to be completed. First, a stable confining potential is required to trap the ions. The calculation of the potential is explained in the previous section. The fabrication of the trap and associated challenges are presented here. In order to prevent collisions with residual gas an ultra high vacuum system with pressure below 10^{-10} mbar is necessary. The possibility of cryogenic cooling of the trap is also discussed. This is an important step in reducing the noise due to surface imperfections leading to ion heating. Finally, a dedicated laser system to address ionization of the atomic barium and cooling of ions are presented in brief.

A. Printed circuit board trap

In this article, we mainly concentrate on printed circuit board (PCB) based ion traps due to their possibility to adopt standard industrial process. However, we will show that the present industry standard is not enough to provide operational traps. The process used to make the design on pcb has been varied from industrial process to in house etching and micro milling. The design of the trap is a five wire geometry with central control electrode surrounded by pairs of RF electrodes to provide trapping potential in the radial direction. While three pairs of DC electrodes are used to drive the central control electrode (V_{CC}), two lateral control electrodes (V_{LC}), and four endcaps (V_{EC}). The very first pcb was made using commercial industrial procedure. The pcb material used is ® *Rogers*3003 because of its superior vacuum compatibility. It consists of 35 μm of copper layer on a 1.5 mm ceramic dielectric substrate. The RF electrode and the central electrode has a width of 350 μm and 250 μm, respectively at the center. The gaps between the electrodes are 200 μm. The trap operating voltage is kept around 200 - 250 V_{RF} at a frequency of 7.2 MHz. The design of this five wire trap geometry is based on both analytical solution as well as CPO simulation. Figure 3 shows a picture of a gold plated pcb trap made by standard industrial technique. Following the simulation process as described in the previous sections, a number of other designs has been experimentally realized. Two stable sets of DC voltages and their corresponding total potential contours for which a stable ion motion is observed is shown in Fig 4.

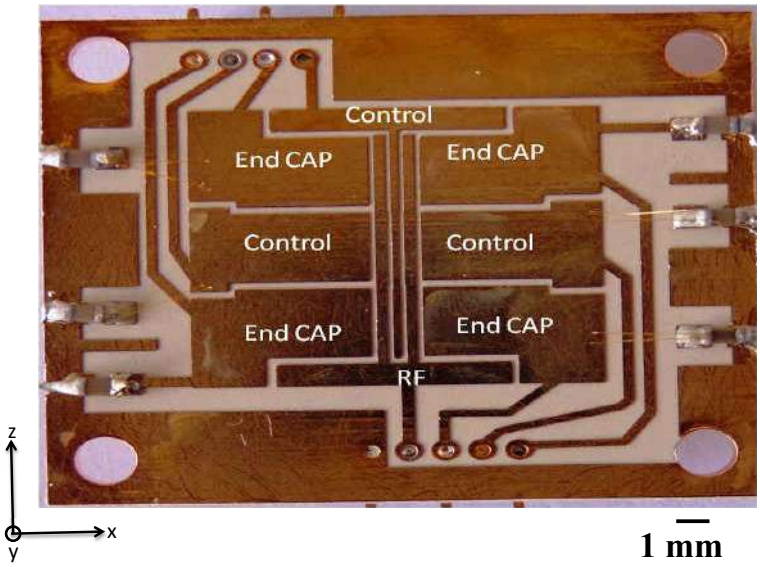


Fig 3. Picture of gold plated trap made by standard commercial technique on PCB. 10nF Capacitors are soldered one end to the ground plane while the electrodes are connected via bonded gold wires to filter induced RF voltage in the DC electrodes.

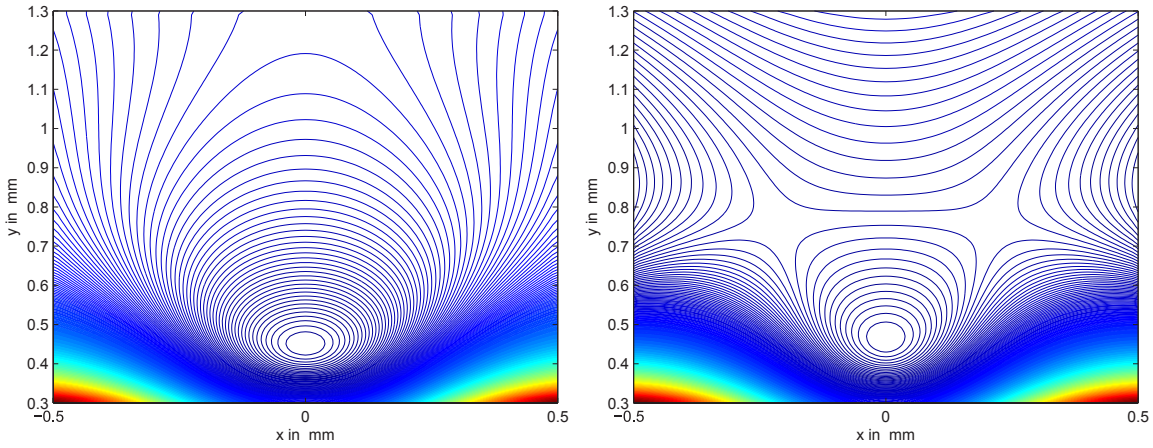


Fig 4. (a) Total pseudopotential cross section obtained for $V_{CC} = 9V$; $V_{LC} = 9.5V$ and $V_{EC} = 10$. (b) Total pseudopotential cross section obtained for $V_{CC} = -3V$; $V_{LC} = -10V$ and $V_{EC} = 5$.

The minimum of the trapping potential also called as the trap center is situated about 400 μm above the surface for the trap described here. This height is mainly determined by the physical dimension of the RF and the central electrodes. Once the RF potential minimum is determined, the next thing needed is to coincide the DC null point with the RF minimal point to confine ion from all three dimensions and more importantly to reduce residual driven or micro motion due to the RF. The DC null point is adjusted by adjusting the voltages set to the DC electrodes as obtained from simulation. Therefore, it is possible to find a set of such voltages for which the two null points coincides.

B. Vacuum Setup

One of the most important requirements for trapping ions is low background pressure. A lower pressure means lower collision rates with the residual gas molecules, hence less probability of ion loss by collisional momentum transfer or chemical reactions. This is even more crucial for surface ion traps due to the inherently low trapping potential in these traps. As we have seen in Sec 2 A, the depth of the potential is only about 100 meV as compared to ≥ 1 eV for a linear trap. Therefore, ion loss for any collision with residual gas at an energy above the trap depth is much high in a surface electrode trap as compared to conventional linear trap. The vacuum chamber which holds the trap is made out of non magnetic stainless steel. The chamber consists of a six-way CF 16 open ports for laser access and barium oven. Two other CF 63 ports perpendicular to the six-way ports are used for fluorescence collection and ion trap support. The trap is mounted on the cold finger connected to the trap support as shown in Figs 5 and 6. The cold finger has a circular cross section with a diameter of 10 mm and a length of 10 mm from the base. Four narrow stands hold the pcb at the same height as the cold finger while the middle part of the pcb stays in contact with the finger. Two other CF 40 ports as observed in Fig 6 serves the purpose of electrical connectivity and vacuum pump connectivity using tees and crosses. The trap stand is custom designed platform attached to CF 63 flange to include the cooling capability using liquid nitrogen or liquid helium. An important characteristic of the whole setup is the scalability and modular design. The setup along with the light injection ports and all mixing optics can be easily transported.

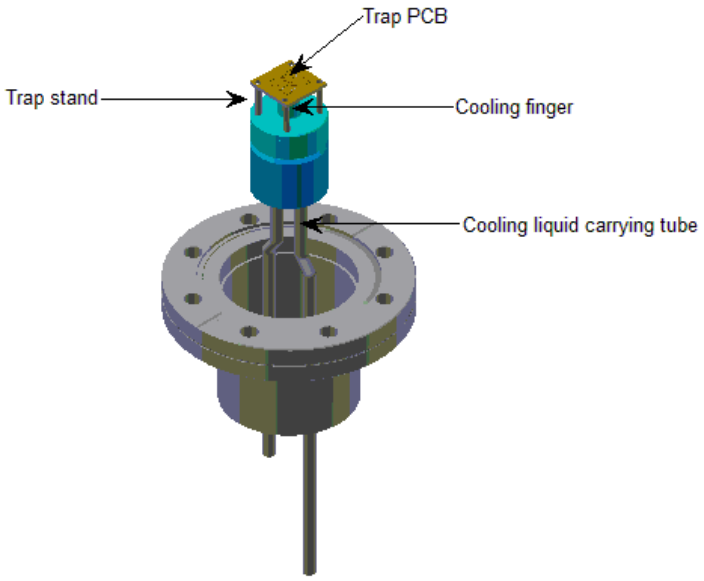
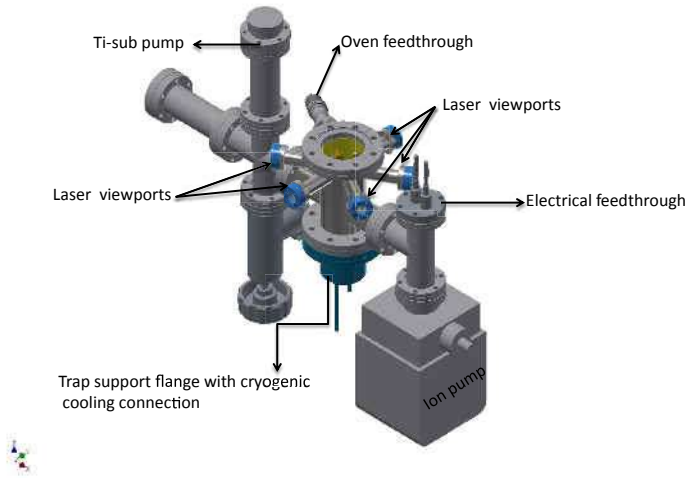


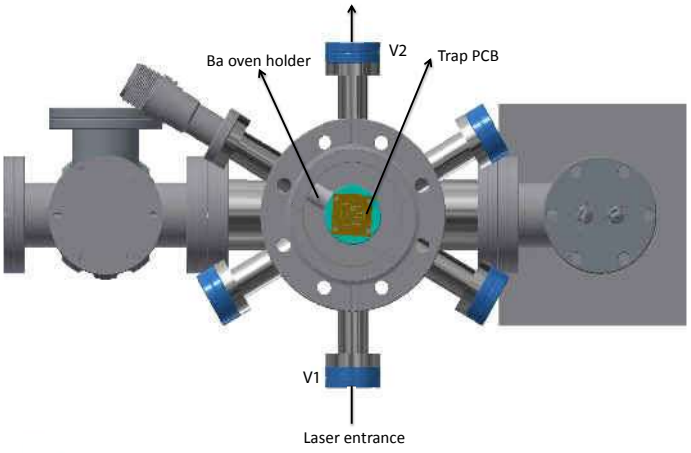
Fig 5. Trap support and cooling finger.

The schematic shown in Fig 7 also indicates the laser direction which grazes the surface trap with the focal point at about 400 μm above the surface. All the lasers are overlapped into a single beam and passes through the trap center (potential minimal point) via the view port V1. Laser beam makes an angle around 20° to 25° with the trap axis which is determined after aligning the oven. This also helps to efficiently cool ions along all three principal axes of the trap. A titanium sublimation pump and an ion pump are connected to the main chamber on either sides of it such that the pressure in the main chamber is not too different from that obtained via the ion pump current reading. Initial pumping of the whole chamber is done via a turbo-molecular pump which is sealed off by an all-metal-valve. Once pumped by the turbo and baked out at a temperature around 120° (limited by the PCB) for a couple of weeks the all-metal-valve is closed and further

pumping is done by the ion pump and the titanium sublimation pumps. The final pressure achieved is around 1×10^{-10} mbar.



(a)



(b)

Fig 6. (a) Schematic of the vacuum setup. (b) Vacuum setup along with laser beam direction.

Now we will discuss the electrical connections of the trap to the external world. All the wires connecting the DC and the RF electrodes are directly soldered to the pcb using no clean solder wires. Induced RF in each DC electrodes is filtered by capacitors directly soldered on the pcb. RF connection is feed via one feed-through connector while all DC voltages are feed through a separate connector. After soldering is done the pcb is cleaned using the following procedure:

1 PCB is immersed in a flux remover Chemtronics ES132 (Flux-O Aqueous Flux Remover) and ultrasonicated at 50° C. Flux remover is diluted with deionized water in a ratio of 1:10. After sonication the pcb is rinsed with de-ionized water and dried.

2 The pcb after being dried is immersed in isopropyl alcohol for 30 minutes in ultrasonic cleaner. It is later de-ionized and let it dry in open.

3 Cleaned and dry pcb is finally put inside the vacuum chamber.

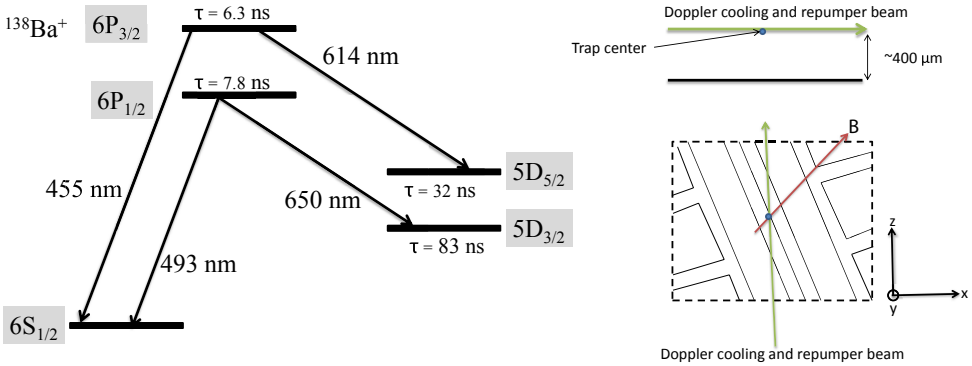


Fig 7. (a) Lowest energy levels of $^{138}Ba^+$ along with the wavelengths of transitions. The 493 nm transition between $6S_{1/2}$ and $6P_{1/2}$ is used for cooling and the laser at 650 nm is used to re-pump the ions out of $5D_{3/2}$ state. (b) Beam direction for doppler cooling and repumper laser with respect to the trap axis and magnetic field direction.

C. Barium oven

Atomic source for barium is an oven consisting of a stainless steel tube of approximate length around 25 - 30 mm. Tantalum wires are spot welded to both ends of the tube for electrical connections. One end of the oven is closed by pinching and covered with a tantalum foil. The barium oven is inserted through one of the six-way ports using a multi-pin feed-through. A macor support is placed through two pins of feed through and other pins are cut short to make space for oven. Barium oven is placed parallel to the pcb surface with the oven opening right above it. This design avoids major barium deposition on the surface. A better design is to have a hole on the central electrode and placing the oven on the back of the trap. However, due to barium vapour deposition during oven operation the hole over time becomes constricted.

D. RF and DC voltage supply

The trap is operated at typical RF amplitude around 250 V producing a trap depth about 120 meV to 250 meV. The supply for the RF needs to be producing stable power output across the trap RF electrodes which can be modeled as capacitor with capacitance of about 15pF. Two separate RF supply has been tested. A resonator made up with lump inductor and capacitors has been constructed to deliver about a maximum of 150 V RF amplitude at 7.2 MHz. The circuit consists of an LC resonator with an impedance matching circuit. Quality factor of about 20 is obtained. Actual voltage delivered to the trap is measured by a 100:1 capacitive divider. Another λ/4 helical resonator has been constructed in order to achieve higher voltage at the trap. The resonator consists of copper wire wounded in helical structure placed inside a cylindrical shield [24]. The signal is feed to trap via a small length BNC connection with sub-c crimps connecting to the connector flange. Voltage generated by a signal generator is amplified by a 2W amplifier and then impedance matched to helical resonator. The exact resonance frequency is tuned observing the reflected signal from trap with a standing wave ratio (SWR) meter connected between amplifier and the resonator. The reflected signal vanishes when the impedance matching is obtained by adjusting the resonator parameters.

The surface trap requires DC voltages of both +ve and -ve polarity. The capacitance between the RF and the Dc electrodes leads to RF noise on the DC electrodes. Since the trap depth is only about 100 eV, it is

absolutely necessary to filter the RF voltage on the DC electrode. Moreover, the DC voltages are required to stable and free of ripples to a level of 10 mV or less. A computer controlled USB supply is used to supply the required DC voltages. The used supply has the advantage of having ten channels each capable of providing both –ve and +ve voltage from 10 V to +10 V with 12-bit resolution. The precision of the DC voltage is about 1 mV. A low pass filter board is placed between the trap and DC supply to filter out any residual high frequency going to the DC electrodes as well as to avoid any trap RF going into the DC supply. Typical filter suppression is around –60 dB. An amplifier at the output of USB supply can be used to supply voltages above 10 V if required at the expense of worsening voltage resolution.

E. Lasers for cooling Barium ion

Barium ion is iso-electronic to alkali atoms with a very simple energy level diagram as shown in Fig 7(a). Only three out of all the laser systems that has been developed compositely to run both the surface trap as well as the other linear 3D ion trap are discussed here due to their relevance to the present work.

The neutral barium atom is resonantly ionized by a single laser while the other two lasers are used for cooling and detection. A home built extended cavity diode laser at 413 nm is used to ionize barium atom via inter combination line of the atom. This allows rather simple single laser resonant ionization of the barium atom as compared to generally used two laser ionization schemes. The details of the laser and ionization has been explained in [25]

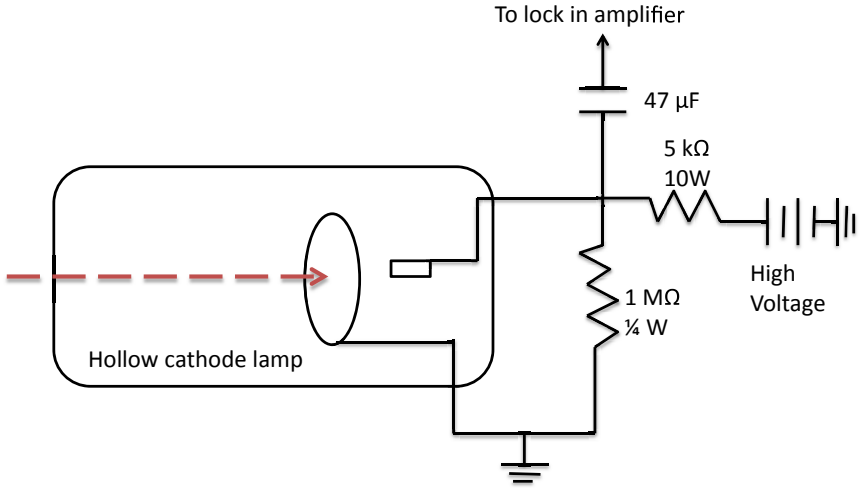


Fig 8. Schematic of opto-galvanic setup. A modulated laser beam at 650 nm used for lock in detection of the small change in current induced by laser.

The strong dipole transition at 493 nm between the levels $6S_{1/2}$ and $5P_{1/2}$ is used for Doppler cooling and fluorescence detection. A frequency doubled module DL-SHG pro from *Toptica* is used for this excitation. Another DL-100 pro from *Toptica* at 650 nm is used as re-pumper to bring the ion population back from the dark D state. Both the lasers are locked to a reference cavity using Pound-Drever-Hall phase locking scheme [26]. The 493 nm is also locked to a atomic reference i.e to a Te_2 reference cell using modulation transfer spectroscopy (MTS) [27]. Similar atomic reference for 650 nm laser is obtained via a barium hollow cathode lamp (HCL) opto-galvanic spectroscopy. In order to have quick reference of the laser wavelengths, all lasers are monitored via a wavelength-meter. The reference cavities of the two cooling lasers are made on a single zerodur block as spacer. This allows very low drift of the cavity reference due to ultra low expansion coefficient of the material, $|\alpha| \leq 10^{-7}\ K^{-1}$. Moreover, using a common zerodur spacer for both the laser reference cavities, it is possible to get rid of the relative drift of the lasers.

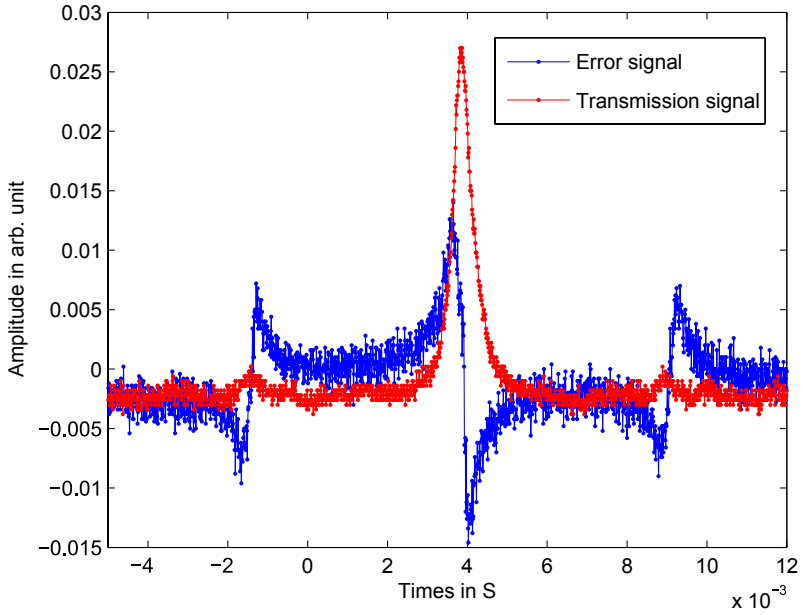


Fig 9. Cavity transmission and error signal as obtained for 986 nm laser. Similar signal is obtained for 650 nm laser as well.

F. Laser injection and imaging

All the cooling and ionization laser lights are individually transmitted from optical table to the trap chamber. These laser lights are then mixed into one beam which is injected into the trap by an achromatic injection lens. So, once they are overlapped only one beam path needs to be controlled. Lasers coming out of the fibers at 493 nm, 413 nm and 650 nm are mixed using dichroic mirrors so that individual polarization can be controlled independently. A flip mirror is placed on the path of the combined beam to monitor the overlap and to fine tune the position of focused light above the pcb surface. The injection/coupling lens as shown in Fig 10 is placed on a x-y-z stage and another pinhole is placed at a distance same as the coupling lens to trap center. The laser beam is first sent above the trap with a very low intensity. The beam is aligned just to graze above the surface which is seen on the CCD camera with a short exposure time. Once the grazing incidence is obtained, the light is reflected by the flip mirror and sent through the pinhole also placed on a x-y-z stage. This serves as the reference height for the trap surface. Now the pinhole is moved by the same height as that of the trap minimum height from surface and the coupling lens is accordingly adjusted using micrometer screws to pass the light through new pinhole position. This alignment is very crucial in order to have the cooling beams overlap with the ion above the surface. Once it is done with care, the flip mirror is moved away from the main path and light is sent through the trap center.

The detection of the ion is performed by collecting the fluorescence light at 493 nm on an electron multiplying charge-coupled device (EM-CCD) camera. In order to improve the signal-to-noise ratio the fluorescence light is collected by a collection lens placed in vacuum and filtered by a narrow band interference filter. To increase the collection effciency it is desirable to have a large solid angle. This is achieved by placing the imaging lens as close to the trap as possible. The collection lens system used has a numerical aperture NA of 0.24 and focal length of 77 mm. The lens is mounted on a x-y-z translational stage. The camera, has an area of 10 mm × 10 mm with a pixel size about 8 μm × 8 μm and a quantum efficiency of about 50% at 493 nm.

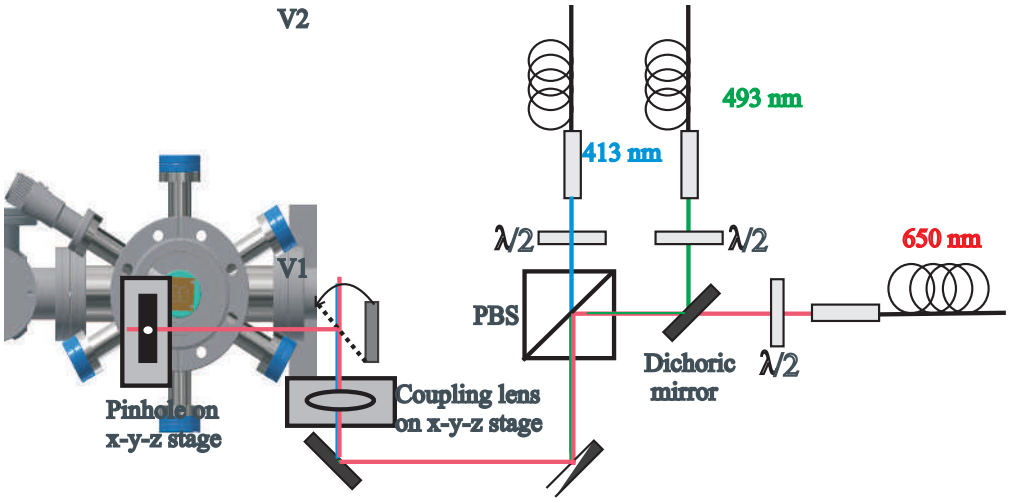


Fig 10. Schematic of the optical setup coupling lasers to the trap. An in-coupling achromatic lens with a focal length of 120 mm focuses the overlapped beam to the trap center. Overlapping of the beams and approximate height of the beam above trap surface can be set by reflecting the light through flip mirror onto a pinhole placed on x-y-z stage.

4 Testing of the surface traps

Four kind of different traps have been tested to trap Ba^+ in several different experiments. These include printed circuit board fabrication made industrially with and without gold deposition on copper. The copper usually oxidizes in air and hence to avoid any such oxidation before the trap is installed in vacuum a thin layer of hard gold is deposited. The other approaches include milling of pcb and etching using our in house facilities. So far, none of the traps has been successful to trap ions in time scales larger than ionization time scales. In the following possible reasons for the non functionality of these traps are discussed along with possible improvements. The major cause of short trapping time for the traps that we have tested and reported here, stems from cold emission from the trap surface due to sharp edges.

After having the trap installed in ultra high vacuum, the supply voltages as well as laser intensities and wavelengths are set to the required values. The DC supply is tested to have very low noise and a precision of less than 1 mV. The RF power delivered to the trap is monitored by the SWR meter reflection being at zero at resonance. Therefore, the only other unknown parameter is actual potential generated by possible non ideal electrodes.

This leads to check the surface quality of the pcb surface as well as the RF breakdown voltage. Issue of breakdown voltage is a common problem in surface electrode ion traps. Typical voltage that can be applied across a gap of around 10 μm is of the order of 100 V. This leads an electric field of about 1×10^6 V/m. The field at the edges can be substantially higher than this value. In our trap designs, the gap between the RF electrodes and the ground are typically around 100 μm to 200 μm.

In order to understand the surface behavior in presence of the RF voltage a test was performed to observe any sign of electrical breakdown on the surface under EM-CCD while RF amplitude of desired value is applied. No breakdown was observed within the applied range of RF voltages. However, sharp and scattered emission points appear as glow on the electrodes edges due to possible electron emissions. The emission intensity at a fixed point as well as the number of emission points are seen to increase with the applied RF voltage after a certain threshold voltage. Gold plated industry made pcb has the lowest threshold

around 110 V across a same gap of 200 μm, while the pcb made via in- house etching process is seen have the threshold voltage around 130 V across a gap of approximately 150 μm. No emission is visible when DC voltage of about 600 V is applied as well as RF voltage applied at atmospheric pressure which rules out the possibility of electrical breakdown. Emission points are seen with EMCCD with a gain of 200 and an acquisition time of 20 s which indicates that the emission is at a very flow rate, however, having electrons emitted from point sources will be accelerated by the applied RF voltage and impinge on the metal surface to generate possible visible emission. Figures 12 and 13 show emission pattern for different kinds of pcb.

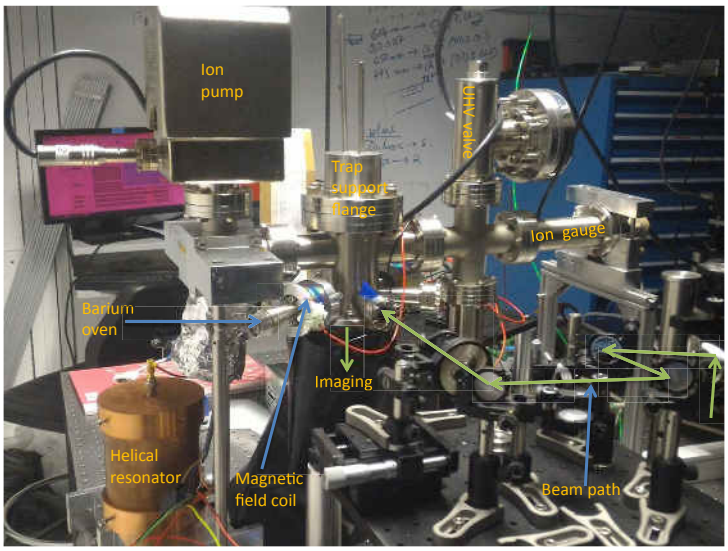
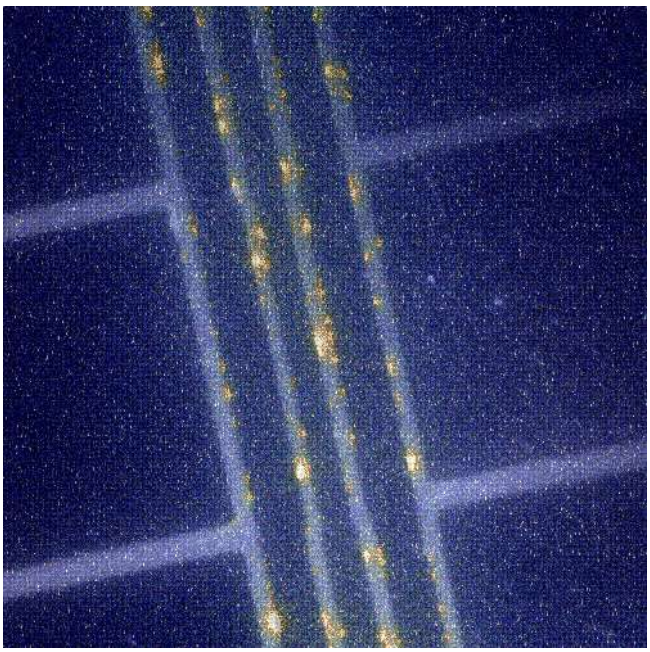
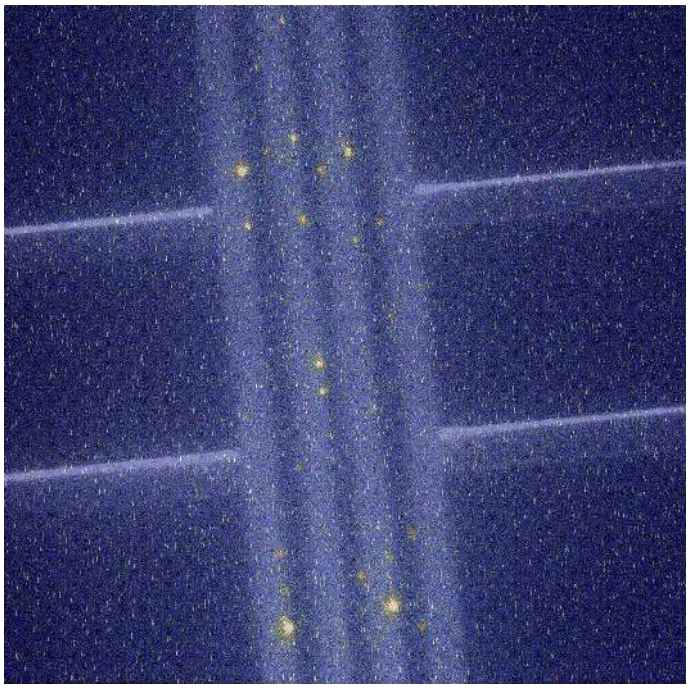


Fig 11. Schematic of the experimental set up.

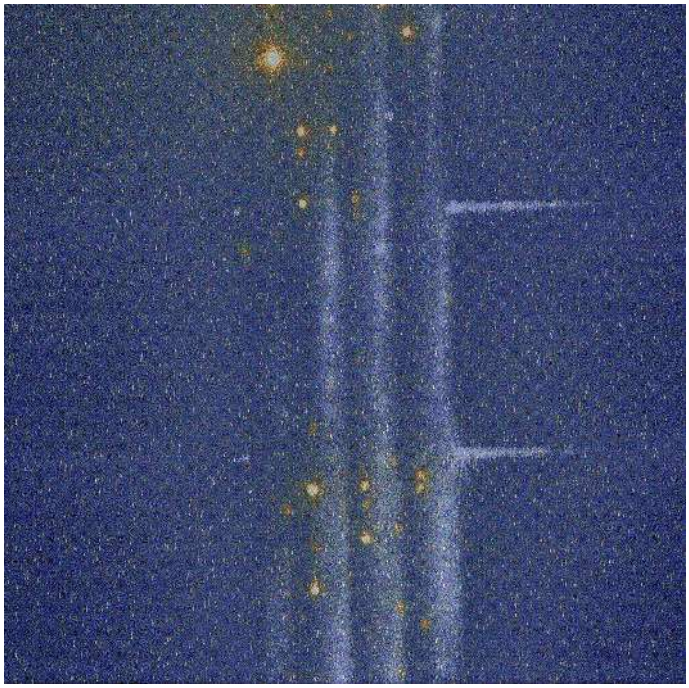


(a)

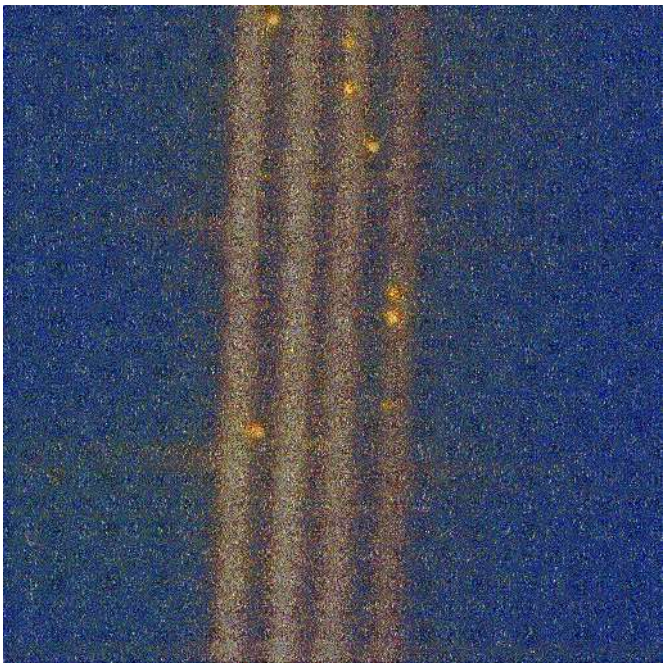


(b)

Fig 12. (a) Field electron emission for pcb from company with gold plated electrodes, (b) Emission pattern for the pcb from company with copper electrodes.



(a)



(b)

Fig 13. (a) Field electron emission from pcb traps made by in- house micro-milling. (B) Emission pattern for pcb made by in- house etching.

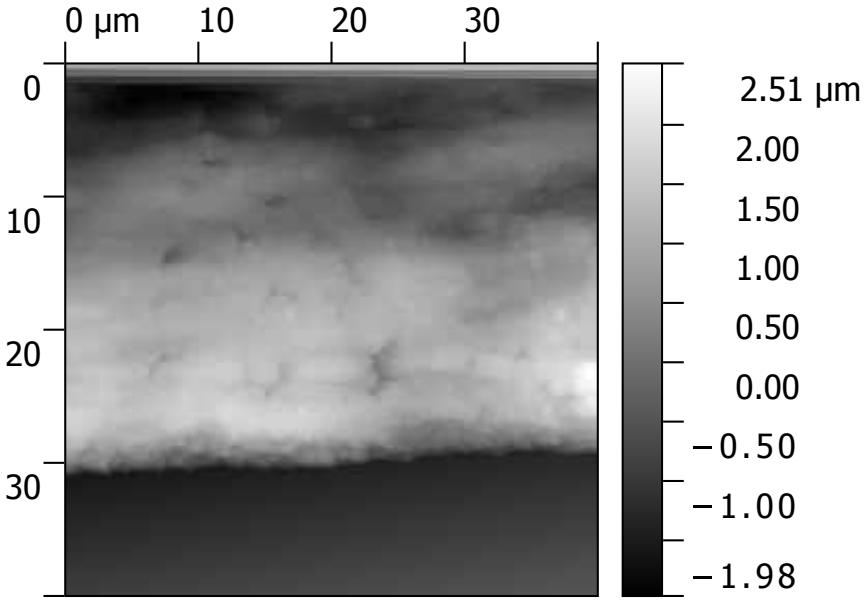


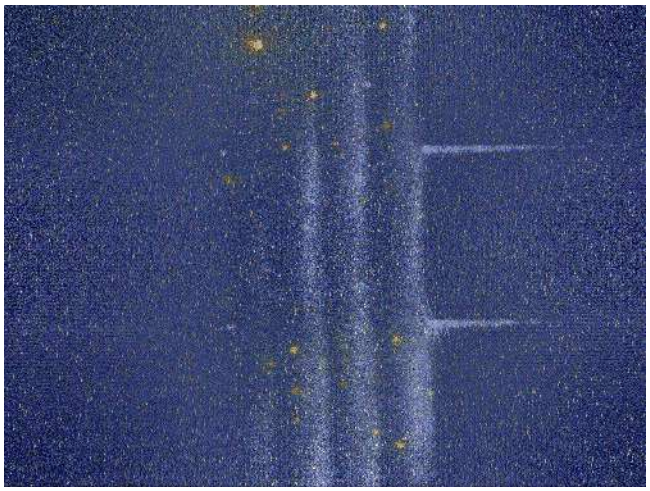
Fig 14. AFM image of the surface of the RF electrode edge containing an emission point.

It was initially believed that these emission points could be associated with some deformation of the edge quality of the electrode. However, the results were not convincing as appeared atomic force microscope

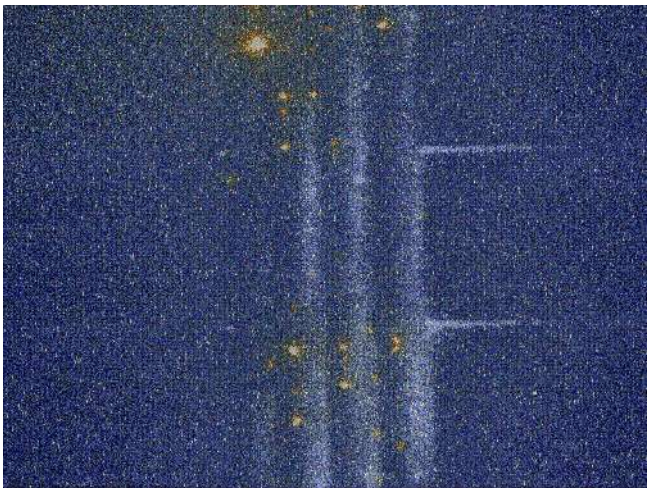
(AFM) image. Only a few points could be associated to sharp edges but similar other points on the edge of the same material showed no emission. Figure 14 shows typical surface profile of RF electrode edge containing emission point as seen with optical microscope and AFM. Similar surface quality is observed even at places where there lies no emission point. Therefore, we looked further into the RF frequency dependence as we already knew that DC voltage showed no emission.

RF frequency dependence

The emission points are seen to increase with the frequency of the RF field. A comparison for the same RF voltage of about 200 V amplitude at a resonance frequency of 4 MHz and 9 MHz shows a clear increase in the number of emission points and their intensities at higher frequencies. Figure 15 shows the comparison of the two pictures taken with 200 gain of CCD and an acquisition time of 20 s. Therefore, the above observations clearly point to the fact that time varying potential is necessary to create the emission points.



(a)



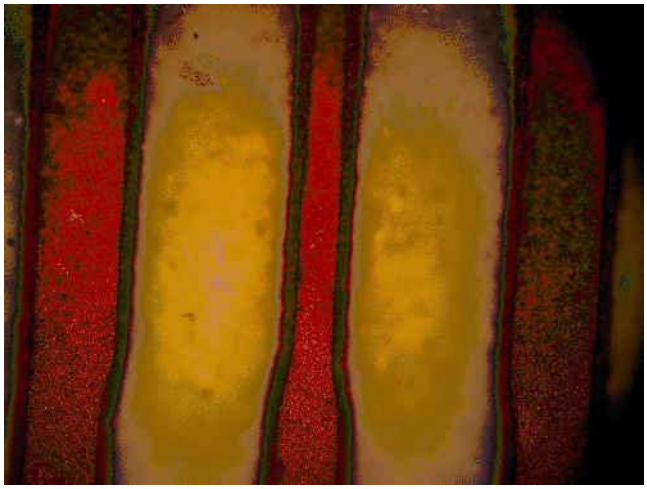
(b)

Fig 15. (a) Field electron emission observed for pcb with copper electrode at RF frequency 4 MHz, (b) Field electron emission observed for pcb with copper electrode at RF frequency 9 MHz.

Effect of electro-polishing

In order to avoid micron size structures the PCB traps were made using in house wet etching technique. They are found to be of relatively better edge quality compared to the industrial made pieces. The electrode pattern was generated on *ROGER 3003* by etching out copper from gaps while holes were made using pcb milling machine. Cold emission has been observed even with these traps. However, the number of points has been significantly lower and only observable above an RF voltage of 130 V. Therefore, to smoothen out the rough edges, electro-polishing of the copper surface has been performed.

(a)

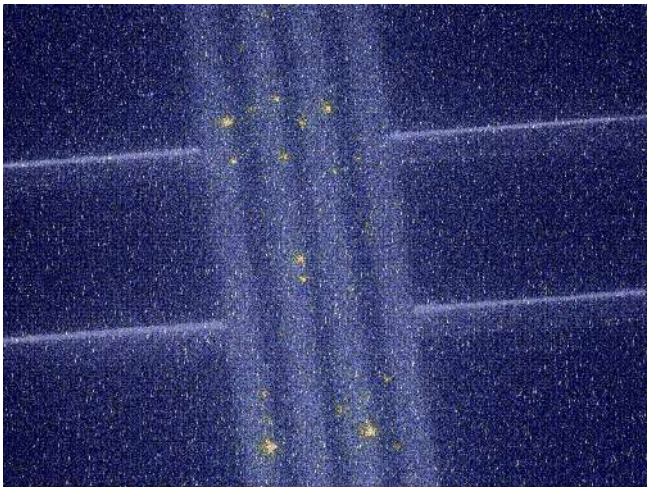


(b)

Fig 16. (a) Microscopic picture of normal pcb trap surface with 20X magnification. The surface contains few patches and sharp points. (b) Microscopic picture of polished pcb trap surface with 20X magnification. The image shows undercut due to longer time of polishing.

Electro-polishing of the copper surface is done by immersing the pcb in an electrolytic solution along with a pure copper (99.99%) block [28]. The solution is prepared using 55% H_3PO_4. The copper block is used as anode and the pcb is used as cathode. Approximately 5 —10 min of polishing time is used. Longer polishing time creates undercut of the copper layer and reduces the width. So an optimized time setting was

used to ensure the width does not change much. The polished pcb obtained are having smoother edges compared to the unpolished edges. Figure 16 shows a comparison of the edges for polished and unpolished traps along with their emission points. This comparative study clearly shows that surface quality specially of the edges is crucial to the fabrication of planar traps.



(a)

(b)

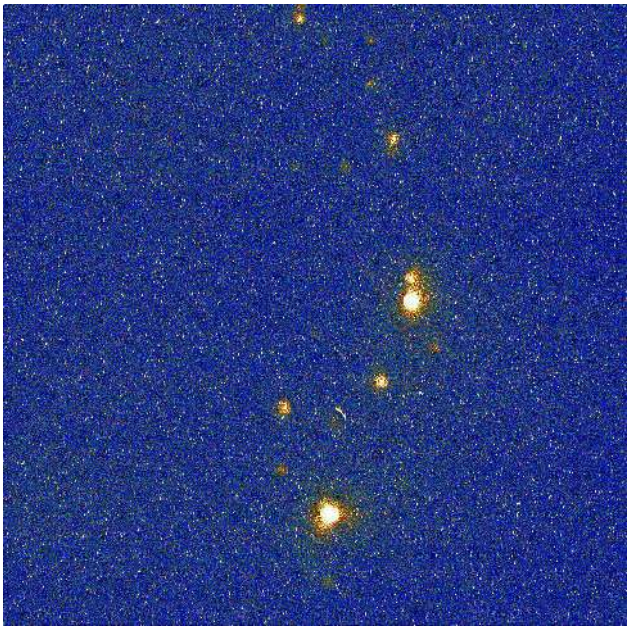
Fig 17. (a) Field electron emission from an unpolished etched surface trap at an RF amplitude of 200V at 9 MHz. (b) Field electron emission from a polished etched surface trap at an RF amplitude of 200V at 9 MHz.

Electron emission points for the polished pcb are seen to be less compared to the unpolished pcb at a fixed RF voltage of 200V and frequency 9MHz, Fig 17. The change in emission threshold for the polished pcb is slightly higher than the unpolished pcb.

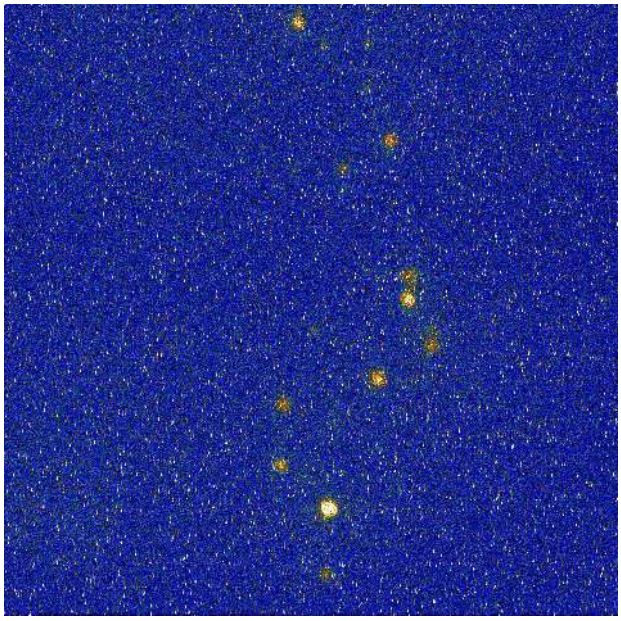
Emission wavelength

It is expected that the emitted wavelength due to electron emission would be mostly in infrared region. A filter glass having 90% transmission bandwidth from 650 nm to 1800 nm has been used in front of

the CCD to observe the wavelength of the light. A large drop in the the intensity of the emission points are visible confirming light emission in visible region below 650 nm or above 1800 nm as well. Since the camera is insensitive to IR light above 1100 nm, the emission is likely to contain a part in the visible spectra below 650 nm which is rather surprising. Figure 18 shows a comparison of the emission with filter and without filter.



(a)



(b)

Fig 18. (a) Field electron emission from a pcb trap without any filter in front of CCD. (b) Field electron emission from a pcb trap with filter FGL 650 in front of CCD.

As a conclusion from our pcb fabricated traps, it was found that the problem of cold electron emission locally distorts the trap potential. Moreover, these electrons due to presence of strong RF field leads to secondary light emission from the copper surface. Even though industrial process are helpful for quick manufacturing of surface traps, the quality of these traps are unacceptable due to rough edges on the electrodes. Furthermore, electro-polishing of the surface clearly reduces the emission points leading to the fact that special care needs to be taken for fabrication of these traps as any such defect will lead to larger heating rates of the ion motion in the trap.

5 Conclusion and outlook

Field electron emission is emission of electrons from solid surface due to high electric fields. This usually refers to electron emission from metallic surface into vacuum. However, it can take place from solid or liquid surface into vacuum, air, fluid or a weakly conducting dielectric as well.

Field electron emission in pure metals occurs at very high electric field of about 1 MV/m which also depends on the work function of the metal. Even though the phenomenon has a number of useful applications in electron microscopy, for surface trap applications it is an undesirable source for dielectric breakdown.

Field electron emission can be explained by quantum tunneling of electrons. Ralph H. Fowler and Lothar Wolfgang Nordheim [29] proposed the theory of field electron emission from bulk materials. In a parallel plate arrangements, the microscopic field F_{M} between the plates is given by

$$F_M = V/W \tag{5}$$

where W is the separation between the plates and V is the applied voltage. Any sharp object created on a plate, makes the local field F at the apex higher than F_M . This can be related to F_M with an enhancement factor γ.

$$F = \gamma F_M \tag{6}$$

The value of γ is determined by the sharp objects shape. So the local field F, which determines the field emission characteristics, higher the value of γ, lower is the value of F_M at which significant emission occurs. Therefore, we believe that emission points observed in our experiment are related to such cold emission points due to the poor surface quality of the industrial process. The traps fabricated by in-house facility showed better quality of surface while elctro-polishing enhanced the quality even better.

Since the industrial process of making these traps are not feasible for any practical use, we have started making traps using metal deposition on sapphire or quartz substrate. A modification in the design also has been brought in the new traps. As the Doppler cooling laser passes parallel to the surface, there will be no projection of the light momentum vector on the $\hat{y}$ axis. So the y-motion will not be cooled. The RF electrodes, therefore, has been made asymmetric to make the RF pseudopotetial tilted from $\hat{y}$ direction [30]. This helps to more efficiently cool the ions in all directions. This also avoids the necessity of keeping the laser beam at an angle to the surface thereby decreasing the scattered background photon number. The tilt can also be generated by few other ways. These include:

1 Addition of a constant offset voltage to all the DC electrodes either left or right side of the trap axis.
2 Extension of the width of DC electrodes on one side as compared to the other side of the RF central electrodes.
3 Splitting the central control electrode in two parts with a tiny gap between them. This is very effective in terms of having a higher tilt that can be generated with lower voltage applied to the electrodes . But at the same time since the central electrode dimension in general is few μm, it becomes more challenging to fabricate it.

The new traps are being prepared using metal deposition on quartz substrate. In one of the fabrication process the trap design in patterned on the quartz substrate by laser cutting. The depth of cut is kept around

200 μm. Thereafter thin layer of Al and Cu is deposited on it. This allows us to keep the surface quality of the polished quartz same as the trap electrodes. Others traps are also being manufactured using gold deposition on quartz substrate. Smaller electrode dimensions and the gap size has been reduced to around 10 μm to increase the trap depth and also more DC electrodes has been added to obtain better control of the axial trap potential. These traps are going to be mounted on a ceramic pin grid array (CPGA) chip carrier and the connections are going to be made by Al wires bonded from CPGA to the trap electrodes. A separate adopter which holds the trap CPGA carrier is soldered to an adapter pcb where all the wires are going to be connected. Figure 19 shows the trap design with electrode dimensions and corresponding RF pseudopotential cross section.//

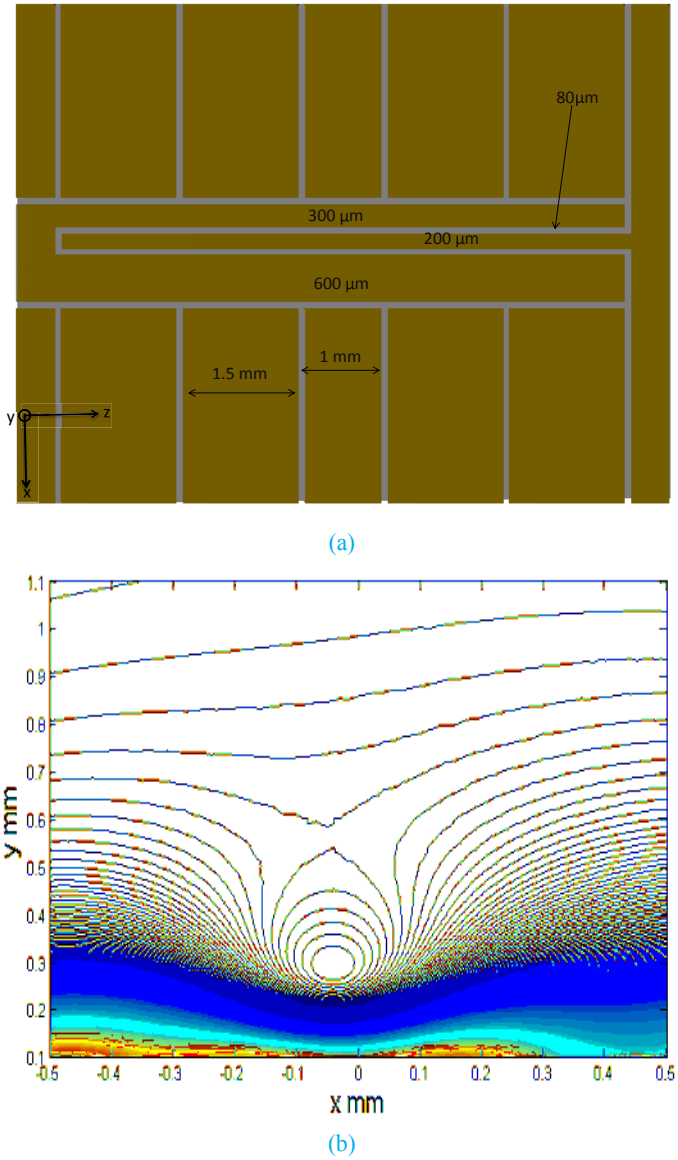


Fig 19. (a) Trap schematic with electrode dimensions. Asymmetric RF electrode dimensions are made to tilt the trap principal axes with the geometric axes. (b) RF pseudo potential contours obtained for the asymmetric trap design. Trap center is situated about 260 μm above the surface.

5 Conclusion

In summary, we have developed an ion trap system which is compact but time consuming in terms of trying out different designs. The fixed wire connections to the adapter pcb allows just to prepare new pcb on CPGA and plug it to the CPGA adapter. The cryogenic cooling ability of the design gives a good prospect to control the heating rates which is crucial in such traps. The challenge of attaining ultra high vacuum is achieved with pcb and solder inside the chamber. Higher atomic mass of barium ion compared to other commonly used species like calcium or strontium makes it difficult in terms of getting narrow electrode widths using pcb milling or etching techniques. A comprehensive study of the field electron emission from RF electrodes is studied at different frequency and amplitude of the applied voltage.

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